

FREQUENCY SYNTHESIZER FOR TV TUNER

Technology: Bipolar

Features:

- o Integrated prescaler $\div 8$ with preamplifier
- o Input frequency max. 1000 MHz
- o Tuning frequency steps 50 kHz
- o 15 Bit programable counter
- o Reference oscillator with 3.2 MHz crystal and $\div 512$ counter
- o Phase detector (reference frequency 6.25 kHz)
- o 4 Programmable band switch driver (open collector)
- o Lock output
- o Microcomputer-controlled via 3-line bus

Case:

20 pin dual inline plastic

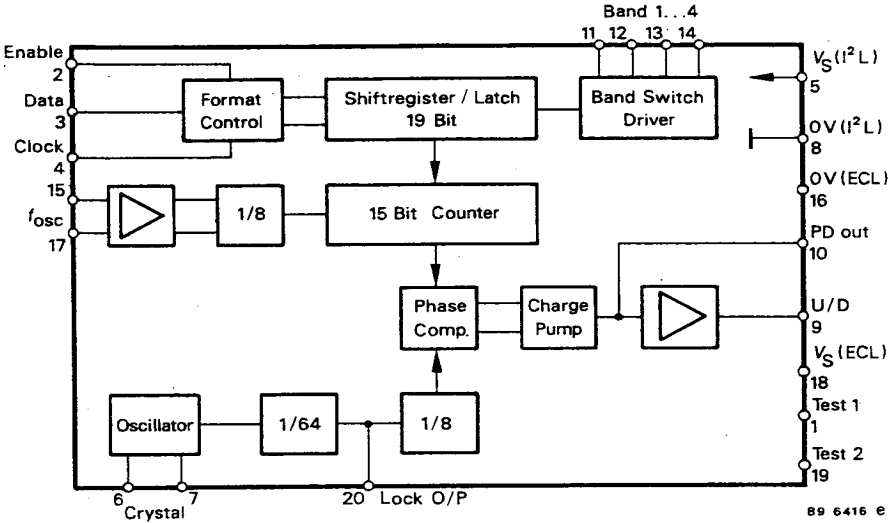
Absolute maximum ratings

Reference point pin 8, 16

Supply voltage	Pin 5,18	V_S	6	V
Input voltage range	Pin 15,17	V_C	0 ... V_S	V
Junction temperature		T_j	125	°C
Ambient temperature range		T_{amb}	-10 ... + 65	°C
Storage temperature range		T_{stg}	-40 ... + 125	°C

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Block diagram

Pin configuration

Pin	Function	Pin	Function
1	Test 1	11	Band 1
2	Enable	12	Band 2
3	Data	13	Band 3
4	Clock	14	Band 4
5	Supply voltage (I^2L)	15	Oscillator input
6	Crystal	16	Ground (ECL)
7	Crystal	17	Oscillator input
8	Ground (I^2L)	18	Supply voltage (ECL)
9	Tuning voltage	19	Test 2
10	Charge pump output	20	Lock output

Electrical characteristics

$V_S = 5\text{ V}$, $T_{\text{amb}} = 25\text{ }^\circ\text{C}$, reference point pin 8,16
unless otherwise specified

				Min.	Typ.	Max.	
Supply voltage	ECL	Pin 18	V_{S1}	4.5	5	5.5	V
	I^2L	Pin 5	V_{S2}	4.5	5	5.5	V
Supply current	ECL	Pin 18	I_{S1}		45		mA
	I^2L	Pin 5	I_{S2}		20		mA
Input sensitivity		Pin 15	V_i		10		mV
Large signal compatibility		Pin 15	V_i	300			mV
Progr. scaling factor			T	1024		32767	
Maximum voltage band switch outputs		Pin 11,12,13,14	V_{max}	12			V
Input level Data, Clock, Enable Test 1,2			V_{IH}	3.0			V
			V_{IL}			0.8	V
Output level (Test mode) Data, Clock			V_{OH}	3.8			V
			V_{OL}			0.5	V

Calculation of the oscillator frequency:

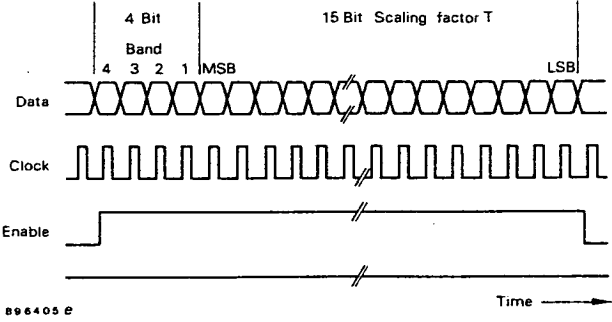
$$f_{\text{osc}} = f_{\text{ref}} \cdot 8 \cdot T$$

f_{osc} : Locked oscillator frequency

f_{ref} : Reference frequency $3.2\text{ MHz}/512 = 6.25\text{ kHz}$

T : Programmable scaling factor

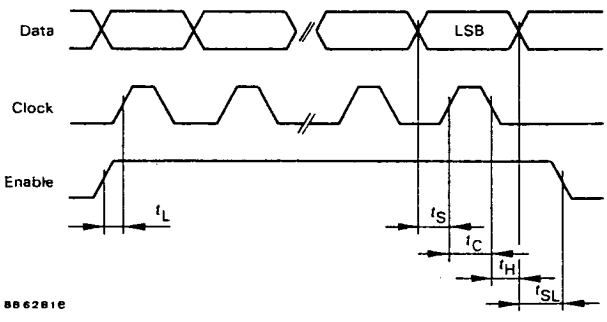
Bus data format

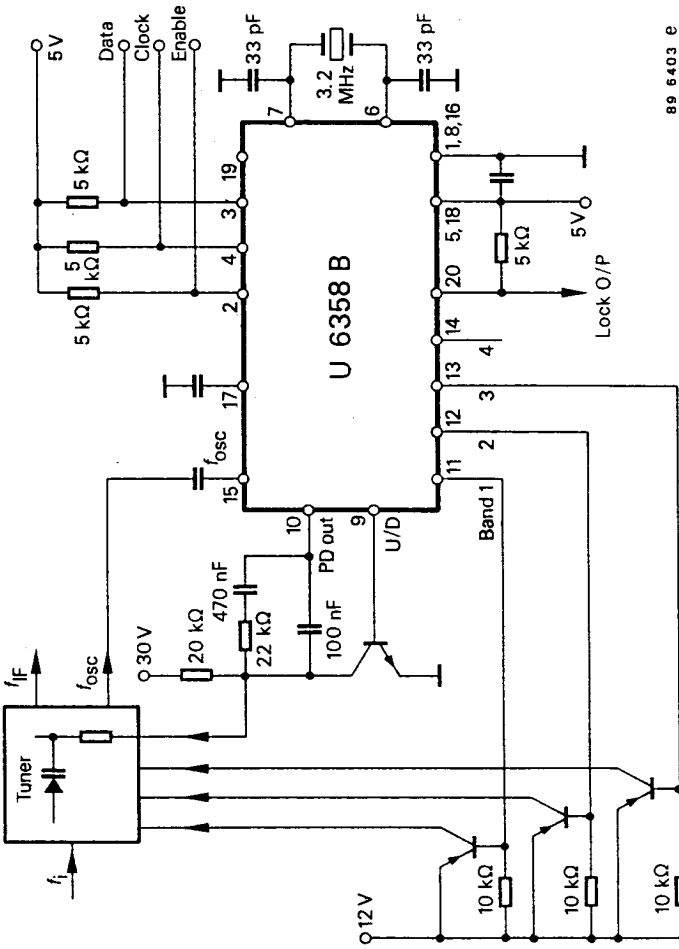


Bus timing

Min. Typ. Max.

Set up time	t_S	2	μS
Enable hold time	t_{SL}	2	μS
Clock "H"-pulse width	t_C	2	μS
Enable set up time	t_L	10	μS
Data hold time	t_H	2	μS





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Application circuit

